

### **REMARKS**

In response to the Office Action dated 11 August 2004, the applicants request reconsideration of the above-identified application in view of the following remarks. Claims 1-25 are pending in the application. Claims 1-23 are rejected, and claims 24 and 25 are objected to. New claims 26-43 will be added, upon entry of the present amendment. No new matter has been added.

#### **New Claims**

New claims 26-43 will be added upon entry of the present amendment. No new matter has been added.

#### **Allowable Subject Matter**

The Office Action indicated that claims 24 and 25 would be allowable if rewritten in independent form. The applicant reserves the right to rewrite claims 24 and 25 in independent form, but believes that all of the claims are allowable in view of the remarks made herein.

#### **Rejection of Claims Under §103**

Claims 1-6, 9-15, and 20 were rejected under 35 USC § 103(a) as being unpatentable over Nishikawa (U.S. 5,805,604) in view of Shichiku et al. (U.S. 6,317,817, Shichiku). The applicant respectfully traverses.

Shichiku issued on 13 November 2001, which is after the filing date of the present application. The applicant does not admit that Shichiku is prior art.

The MPEP requires that a suggestion and a reasonable expectation of success be provided for a rejection based upon multiple references under 35 USC § 103:

“To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.”<sup>1</sup>

The suggestion or motivation to combine references and the reasonable expectation of success must both be found in the prior art.<sup>2</sup> The MPEP refers to “the importance of relying on objective evidence and making specific factual findings with respect to the motivation to combine references.”<sup>3</sup>

Nishikawa relates to an apparatus for reading and writing data including a rearranging circuit that rearranges bits of data having different significances when a region of a memory circuit has a defective portion. The Office Action states that “Nishikawa does not explicitly discard the least significant bit... respective bits are rearranged so that the LSC is stored in the defect region.”<sup>4</sup>

Shichiku relates to an image operation processing apparatus storing discrete data.<sup>5</sup> Shichiku describes a method of storing data where “least significant bits are discarded.”<sup>6</sup> The purpose of this method is to store data densely at continuous addresses instead of discretely. This method uses memory efficiently.<sup>7</sup>

The Office Action improperly combines Nishikawa and Shichiku according to the following reason:

“it would have been obvious ..... to improve upon the image operation processing apparatus, as disclosed by Shichiku. By doing so, it is possible to store data of the results of operation in continuous address of the memory, enabling efficient use of the memory areas.”<sup>8</sup>

The Office Action has not shown evidence of a reasonable expectation of success of this combination. Nishikawa stores the LSB in a memory defect region.<sup>9</sup> Nishikawa is storing data

---

<sup>1</sup> MPEP 2143.

<sup>2</sup> MPEP 2143.

<sup>3</sup> MPEP 2143.01.

<sup>4</sup> Office Action, page 2.

<sup>5</sup> Shichiku, Title.

<sup>6</sup> Shichiku, Col. 9, line 51.

<sup>7</sup> Shichiku, Col. 9, line 57 to Col. 10, line 4.

<sup>8</sup> Office Action, page 3.

<sup>9</sup> Nishikawa, Col. 6, lines 4-16.

bits in a memory with defect regions. Shichiku discards least significant bits to store data densely at continuous addresses. If this method is used in Nishikawa, then important data will be stored in the defect regions of the memory used in Nishikawa. The data that Shichiku is storing will be corrupted by having some bits stored in defect regions. The Office Action has not presented evidence that this combination of Nishikawa and Shichiku has a reasonable expectation of success. Specifically, the Office Action has not shown evidence that the method Shichiku can be implemented successfully with data corrupted by the defect regions in the memory of Nishikawa.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 1-6, 9-15, and 20 has not been established in the Office Action, and that claims 1-6, 9-15, and 20 are in condition for allowance.

Claims 7, 8, 16-19, and 21-23 were rejected under 35 USC § 103(a) as being unpatentable over Nishikawa and Shichiku, and further in view of Kondo (U.S. 5,153,574). The applicant respectfully traverses.

Kondo relates to an interface for a thin display panel having a timing circuit.<sup>10</sup> Kondo describes the use of timing signals, and shows RAM memories with control circuits used to store color data. The Office Action does not assert that Kondo provides a reasonable expectation of success of a combination of Nishikawa and Shichiku that is missing in the Office Action. Therefore, the Office Action has not shown that Nishikawa, Shichiku, and Kondo together support a *prima facie* case of obviousness of claims 1-6, 9-15, and 20.

The Office Action also does not identify a sufficient suggestion for combining Nishikawa and Shichiku with Kondo. The Office Action states the following:

“It would have been obvious to use the memory defect routing of Nishikawa in a LCD display system with three memories for color display. This would have been obvious as suggested by Nishikawa wherein Nishikawa’s device is used for image data, “A rearranging circuit 12 has a function to rearrange respective bits representing image data...” col. 5, and lines 40-41 of Nishikawa.”<sup>11</sup>

---

<sup>10</sup> Kondo, Abstract.

<sup>11</sup> Office Action, page 5.

Although both Kondo and Nishikawa may store image data in memory devices, this is completely irrelevant to the technical combination proposed in the Office Action, which involves memory defect routing. The end use that stored data is put to (an image in the instant case) has no bearing on how that data is stored in a memory device, and the method of storing the data does not affect the resulting image.

No suggestion or motivation for combining Kondo with Nishikawa and Shichiku can be found in the references themselves. Kondo does not describe the inner-workings of the RAM memories, and in particular does not describe how the RAM memories compensate for defective cells. RAM memories are commercially available, and the inner-workings of such a RAM memory does not need to be known for Kondo to have a complete description. The RAM memories in Kondo are “black boxes” with inputs and outputs. Although Nishikawa has stated that its methods can be used with a RAM memory, the Office Action has not provided evidence that the inner-workings of the RAM memory shown in Kondo could be operated according to the method of Nishikawa. The Office Action has not provided evidence that the RAM memory shown in Kondo does or does not have a method to compensate for defective cells. Therefore, there is no evidence of a suggestion for the technical combination set forth in the Office Action. Given that Kondo does not discuss the inner-workings of the RAM memory devices, the Office Action has also not shown evidence of a reasonable expectation of success of applying the method of Nishikawa to manage defective cells in the RAM memory devices of Kondo.

The Office Action states:

“Further, since Nishikawa is directed at providing a method and apparatus to mitigate memory defects without requiring the extra overhead of spare memory, it would have been obvious to include the rearranging circuits (i.e., rerouting circuitry) to the device of Kondo so as not to require extra memory and to require a change in the size of the memory. As combined, the system of Kondo and Nishikawa would simply add the input rearranging circuits 12 (first repair router) of Nishikawa to each of the inputs of memories 211, 212 and 213 of Kondo and add the output rearranging circuits 13 (second repair router) of Nishikawa on the outputs of memories 211, 212, and 213 of Kondo”..... “the use of a reflective electrode is well known in the art and would be obvious to use in a liquid crystal device without a back-light, i.e., these type of LCD

displays are typical in watches or front lit displays, examiner will provide references if desired.”  
<sup>12</sup>

The Office Action did not cite any evidence in Nishikawa, Shichiku or Kondo or any other prior art supporting the statements in the above-quoted paragraphs as is required by MPEP 2143. The Office Action has not established a motivation to combine Nishikawa and Shichiku with Kondo, or a reasonable expectation of success, based on these statements.

The Examiner offered to provide references. A *prima facie* case of obviousness has not been established with the applied references Nishikawa, Shichiku, and Kondo. A simple addition of more references will not support a *prima facie* case of obviousness without evidence of a suggestion for the combination of these references and evidence of a reasonable expectation of success.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 7, 8, 16-19, and 21-23 has not been established in the Office Action, and that claims 7, 8, 16-19, and 21-23 are in condition for allowance.

---

<sup>12</sup> Office Action, page 5.

**CONCLUSION**

The applicants respectfully submit that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.


If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SAMSON X. HUANG

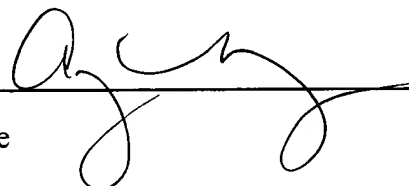
By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
Attorneys for Intel Corporation  
P.O. Box 2938  
Minneapolis, Minnesota 55402  
(612) 373-6973

Date 12 November 2004 By   
Robert E. Mates  
Reg. No. 35,271

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 12th day of November, 2004.

Amy Moriarty  
Name

  
Signature